ABSTRACT

An apparatus comprising three sampling circuits to sample incoming data and a quarter clock. A clock generation unit is included to generate at least three sampling clocks from a local clock. Each of the three sampling clocks are configured to sample the incoming data and the quarter clock. A phase detector is also included to detect a phase difference between the quarter clock and the local clock and to generate a recovered quarter clock. A delay line is further included to delay the sampled incoming data and the recovered quarter clock by the detected phase difference.